AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

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1. (CURRENTLY AMENDED) An apparatus comprising:

a first circuit configured to ~~wake up a second circuit~~ present any of a plurality of divided delay signals as a wake-up signal in response to an input signal; and

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a second circuit configured (i) to exit a suspend or sleep mode in response to said wake-up signal and (ii) to generate said input signal, wherein said input signal comprises a programmable delay value.

2. (ORIGINAL) The apparatus according to claim 1, wherein said input signal comprises a user programmable signal.

3. (ORIGINAL) The apparatus according to claim 1, wherein said input signal comprises a multi-bit signal.

4. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein said programmable delay value is determined by said apparatus in response to one or more firmware instructions.

5. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein said programmable delay value comprises a wake-up delay timing value.

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6. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said first circuit comprises:

a delay circuit configured to ~~present~~ generate a ~~first~~ delay signal; and

a select circuit configured to (i) generate said plurality of divided delay signals and (ii) present ~~a second delay~~ said wake-up signal in response to said ~~first~~ delay signal and said input signal~~, wherein said second delay signal is configured to wake up said second circuit~~.

7. (CURRENTLY AMENDED) The apparatus according to claim 6, wherein said input signal is configured to control ~~a programmable delay of~~ selection of one of said plurality of divided delay signals for presentation as said ~~second delay~~ wake-up signal.

8. (CURRENTLY AMENDED) The apparatus according to claim 7, wherein each of said ~~programmable~~ divided delay signals has a period that comprises a multiple of a ~~delay~~ period of said ~~first~~ delay signal.

9. (CURRENTLY AMENDED) The apparatus according to claim 6, wherein said select circuit is ~~further~~ configured to ~~select one of a~~ multiplex said plurality of ~~third~~ divided delay signals in response to said input signal.

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10. (CURRENTLY AMENDED) The apparatus according to claim 6, wherein said select circuit comprises:

a divider circuit configured to ~~present one or more~~ generate said plurality of divided delay signals in response to said ~~first~~ delay signal; and

a multiplexer configured to present said ~~second delay~~ wake-up signal in response to said ~~one or more~~ plurality of divided delay signals and said input signal.

11. (CURRENTLY AMENDED) The apparatus according to claim ~~6~~ 1, wherein said ~~select~~ first circuit comprises a counter configured to generate each of said ~~second~~ plurality of divided delay ~~signal~~ signals in response to a different value of said input signal ~~and said first delay signal~~.

12. (CURRENTLY AMENDED) The apparatus according to claim 6, wherein said delay circuit is further configured to present said ~~first~~ delay signal in response to an enable signal.

13. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said input signal is generated in response to a ~~device selected from the group consisting of input pins, data pins, microprocessor code, and firmware~~ value stored in a register of said second circuit.

14. (CURRENTLY AMENDED) An apparatus comprising:

a first circuit configured to operate in a sleep mode and a wake-up mode; and

a second circuit configured to control switching of said first circuit from said sleep mode to said wake-up mode after a programmable period of time, wherein said second circuit comprises (i) a delay block configured to generate a delay signal in response to an enable signal and (ii) a divider circuit configured to generate a plurality of divided delay signals in response to said delay signal, where said divided delay signals determined a range of said programmable period of time.

15. (CURRENTLY AMENDED) A method for adjusting wake-up timing comprising the steps of:

(A) receiving an input signal from a circuit; ~~and~~

(B) generating a delay signal;

(C) generating a wake-up signal by dividing said delay signal according to a value of said input signal; and

(D) waking-up ~~a~~ said circuit ~~after a delay time determined~~ in response to said ~~input~~ wake-up signal, wherein said input signal comprises a programmable delay value.

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16. (PREVIOUSLY AMENDED) The method according to claim 15, wherein said input signal comprises a user programmable signal and said programmable delay value comprises a wake-up timing value.

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17. (PREVIOUSLY AMENDED) The method according to claim 15, wherein said programmable delay value is determined in response to execution of one or more computer executable instructions stored in a computer readable medium.

18. (CURRENTLY AMENDED) The method according to claim 15, ~~wherein step (B)~~ further ~~comprises~~ comprising the ~~sub-steps~~ steps of:

~~(B-1) presenting a first~~ generating a plurality of divided delay signals in response to said delay signal; and

~~(B-2) presenting a second~~ selecting one of said divided delay signals as said wake-up signal in response to said ~~first delay signal and said~~ programmable delay value~~, wherein said second delay signal is configured to wake-up said circuit~~.

19. (CURRENTLY AMENDED) The method according to claim ~~18~~ 15, wherein step ~~(B)~~ (C) further comprises the sub-step of:

~~(B-3) controlling a programmable delay of said second delay signal~~ programming a counter in response to said programmable delay value and clocking said counter in response to said delay signal.

20. (CURRENTLY AMENDED) The method according to claim 15, further comprising the step of:

~~(C) generating~~ adjusting said value of said input signal in response to a comparison of a measured wake-up delay to a predetermined wake-up delay.

21. (PREVIOUSLY ADDED) The apparatus according to claim 1, wherein said first and second circuits are implemented on a single integrated circuit.

22. (PREVIOUSLY ADDED) The apparatus according to claim 1, wherein (i) said first circuit is configured to periodically wake up said second circuit and (ii) a sleep period of said second circuit is determined by said programmable delay value.

23. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said second circuit is configured to ~~generate~~ adjust

said programmable delay value of said input signal in response to a comparison between a predetermined wake-up time and a measured wake-up time.

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24. (CURRENTLY AMENDED) The method according to claim 15, further comprising:

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setting an initial value for said programmable delay value;

enabling a wake-up delay timer configured to generate ~~a~~ said wake-up signal in response to said programmable delay value;

measuring a delay time of said wake-up timer; and

adjusting said programmable delay value in response to a result of comparing said measured delay time with a predetermined wake-up delay time.

25. (PREVIOUSLY ADDED) The apparatus according to claim 14, wherein said second circuit is configured to determine said programmable period of time in response to an input signal comprising a programmable delay value.